Attorney Docket # 5367-144PUS

MS-AF

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Jörg SORG et al.

Serial No.: 10/519,347

Filed: June 20, 2004

For: Surface-Mountable Light-Emitting Diode and/or Photodiode and Method for the Production thereof

Examiner: Tran, Thanh Y.
Group Art: 2892

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Signature

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Date of Signature

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

SIR:

This is a Request for a Panel Review of Issues on Appeal in accordance with the Office Gazette Notice dated July 12, 2005. The present request is filed concurrently with a Notice of Appeal. No amendments are being filed with this request. Arguments supporting the Request begin on page 2 of the present communication.

REMARKS

This Notice of Appeal and Request is being filed in response to the Final Office Action dated October 16, 2008. The issues for review are: whether claims 1 and 3 are anticipated by U.S. Patent No. 6,107,678 ("Shigeta"); whether claims 6-8, 10, and 11 are obvious over Shigeta; whether claims 9, 12, and 16-18 are obvious over Shigeta in view of U.S. Patent No. 3,781,596 ("Galli"); and whether claims 13-15 and 19 are obvious over Shigeta in view of Galli, and further in view of U.S. Patent No. 4,812,421 ("Jung").

Rejection of independent claim 1 under 35 U.S.C. §102(b)

The Examiner's rejection of independent claim 1 as anticipated by Shigeta is clearly improper because it is based on an error in interpreting the Shigeta reference. As will be described in more detail below, Shigeta does not disclose a semiconductor chip mounted in openings in the plastic film 106. In contrast, the only chip 115 disclosed by Shigeta is mounted on a side of a lead frame 113 opposite the film 106 and can not be considered to be mounted in an opening in the film 106.

Applicants' independent claim 1 specifically recites a surface-mountable miniature luminescent diode or photodiode that includes, inter alia, "a semiconductor chip ... which comprises a first contact area, a second contact area", "a plastic film arranged on, and connected to, the metal foil, the plastic film defining a plurality of openings in regions arranged on the first and the second chip connection regions", and "wherein the semiconductor chip is mounted in one of the plurality of openings of the plastic film with the first contact area contacting the first chip connection region."

Applicants' recited invention is directed to a surface-mountable miniature luminescent diode or photodiode where the components are arranged in the following order: a metal foil 12, then a plastic film 14 with openings 34, 36, and then a semiconductor chip 22, which is mounted on the metal foil 12 in an opening 34 of the plastic film 14 (see Fig. 1 of Applicants' specification).

Shigeta discloses a lead frame with a reinforcing ring surrounding a semiconductor element, which is electrically connected to leads through electrodes. According to Shigeta, a lead frame is first formed without a semiconductor chip and then a semiconductor package is formed by mounting the lead frame on a semiconductor chip (see Abstract of Shigeta).

The Examiner cites Figs. 10E-10H of Shigeta as teaching Applicants' recited invention. Specifically, the Examiner asserts that Figs. 10E-10H show a semiconductor arranged on, and in electrical contact with, a leadframe 113/105, and that the terminals 110 are the connection regions for the semiconductor. The Examiner further asserts that the insulating film 106 and the conductor pattern 105 of Shigeta correspond to Applicants' recited plastic film disposed on a metal foil, and that the semiconductor chip is mounted in one of the plurality of openings of the plastic film 106 with the first contact area contacting the first chip connection region 110. Applicants' disagree and submit that the Examiner has misinterpreted Shigeta.

According to Shigeta, Figs 10A-10H illustrate steps during a manufacturing process of a lead frame 113, in which a chip is not yet attached (see col. 11, lines 35-37 of Shigeta). The lead frame 113 includes a metal base 101 formed by disposing an aluminum film 103 and a nickel film 104 on a substrate 102 (see col. 10, lines 6-10 of Shigeta). A plurality of lead patterns 105 are then formed on the surface of the metal base 101 (see col. 10, lines 29-35 of Shigeta). An insulating film 106 is laminated on the lead pattern 105 to form a wiring film 107 and a number of holes 108 are formed in the insulating film 106 (see Fig. 10D and col. 10, lines 44-52 of Shigeta). Leads 109 extending from the pattern 105 are formed as the connection portions to the electrode pads of the semiconductor chip (see Figs. 10F-H, 11A, and 11B, and col. 10, lines 53-59 of Shigeta).

External connection terminals 110, which include solder balls, are formed at the termination of the lead patterns 105 coated with the insulating film 106 (just above the holes 108) by using the insulating film 106 as a mask (see Fig. 10E and col. 11, lines 3-14 of Shigeta). The layers 102, 103, 104 of the metal base 101 are selectively removed leaving an outer ring 111 connected to the wiring film 107 (see Figs. 10F-10G and col. 11, lines 60-65 of Shigeta).

Fig. 11A of Shigeta shows attachment of a semiconductor chip 115 to the lead frame 113, on a back surface side of the wiring film 107 through an adhesive layer 114 (see Fig. 11A and col. 11, lines 38-44 of Shigeta). The chip 115 can not be considered to be mounted "in one of the plurality of openings of the plastic film", as recited in independent claim 1.

Thus, the Examiner's rejection of claim 1 is in error because none of the Figs. 10E-10H cited by the Examiner show a semiconductor chip. Furthermore, since the semiconductor chip 115 disclosed by Shigeta is arranged on a side of the lead patterns 105 facing away from the insulating film 106, Shigeta fails to disclose, teach or suggest "wherein the semiconductor chip is mounted in one of the plurality of openings of the plastic film with the first contact area contacting the first chip connection region", as expressly recited in independent claim 1.

Further, the connection terminals 110 do not, and are not intended to, connect to any semiconductor chip. The connection terminals 110 are "solder balls" disposed at the end of lead patterns 105 and formed over the holes 108. Furthermore, the connection terminals 110 are the external connections of the package for connection to a printed circuit board or the like. Therefore, terminals 110 of Shigeta do not in any way correspond to Applicants' recited first and second chip connection regions.

Moreover, there is nothing in the disclosure of Shigeta that teaches or suggests that the semiconductor chip is a "surface-mountable miniature luminescent diode or photodiode" that includes "at least one of an active, radiation-emitting region and radiation-receiving region", as recited in Applicants' claim 1.

Additionally, as discussed above, Applicants' invention is concerned with reducing the overall height of the device. According to Applicants' invention, only the thicknesses of the semiconductor and the metal foil contribute to the overall height of the device. The thickness of the plastic film does not contribute to the overall height because of the semiconductor being disposed in an opening in the plastic film (see Fig. 1 of Applicants' published specification).

Shigeta, in contrast to Applicants' invention, is not at all concerned with reducing the overall height of the device. This is evidenced by the device of Shigeta including layers (e.g., the adhesive layer 114) in addition to the metal layer, the semiconductor, and the film layer that increase the overall height of the device.

For all the above reasons, Shigeta necessarily fails to teach or suggest "a plastic film arranged on, and connected to, the metal foil, the plastic film defining a plurality of openings in regions arranged on the first and the second chip connection regions", "wherein the semiconductor chip is mounted in one of the plurality of openings of the plastic film with the first contact area contacting the first chip connection region", as recited in Applicants' claim 1. Accordingly, claim 1 is patentable over Shigeta under 35 U.S.C. §102(b).

Claims 3 and 6-11, which depend from independent claim 1, incorporate all of the limitations of independent claim 12 and are, therefore, deemed to be patentably distinct over the cited references for at least those reasons discussed above with respect to independent claim 1.

Claim 12 has recites limitations similar to claim 1, which Shigeta fails to teach or suggest. Galli fails to teach or suggest what Shigeta lacks. Therefore, claim 12 is deemed to be patentably distinct over Shigeta and Galli for at least those reasons discussed above with respect to independent claim 1.

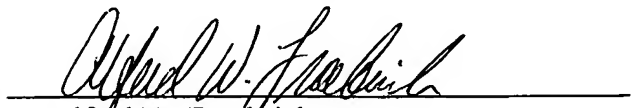
Claims 13-19, which depend from independent claim 12, incorporate all of the limitations of independent claim 12 and are, therefore, deemed to be patentably distinct over the cited references for at least those reasons discussed above with respect to independent claim 12.

Conclusion

In view of the above remarks, the rejection of Applicants' claims should be withdrawn.

If any additional fees are required at this time in connection with the present application, they may be charged to our Patent and Trademark Office Deposit Account No. 03-2412

Respectfully submitted,
COHEN PONTANI LIEBERMAN & PAVANE LLP

By 

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